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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,594	09/30/2003	Rainer Hoehler	10808/95	9938

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EXAMINER	
YOHA, CONNIE C	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 04/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,594	HOEHLER, RAINER	
	Examiner	Art Unit	
	Connie C. Yoha	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Connie C. Yoha

CONNIE C. YOHA
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/18/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 2/18/05 was considered.

2. Claims 1-34 are presented for examination.

Drawings

3. The drawings are objected to because of the following minor informalities:

Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP э 608.02(g).

Correction is required.

Claim Rejections - 35 USC э 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1-6, 8-10, 12-16, 18-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Takemae et al, Pat. No. 6349067.

With regard to claim 1 and 21, Takemae discloses a memory control system comprising: an inherent memory controller; a memory device (fig. 4) inherently connected to the memory controller via a command bus, wherein command signals are

directed from said memory controller to said memory device (it is inherently known in the semiconductor memory art that in every memory system there must be a memory controller controlling the operation of the memory device through the use of a memory controller bus to communicate between the memory controller and the memory device), wherein the memory device comprising: one or more memory banks (fig. 4, 9); a row address register (fig. 4, 61a); a command decoder (fig. 4, 2) that is connected to said row address register (fig. 4, 61a), and receives said command signals (fig. 4, for example /CS, /RAS, /CAS and /WE) and controls the contents of the row address register; and a refresh circuit (fig. 4, 4 and 7a) connected to said one or memory banks and said row address register, wherein said refresh circuit avoids unnecessary power consumption for refreshing said one or more memory banks (col. 1, line 58-62).

With regard to claim 2 and 22, Takemae discloses wherein said refresh circuit only refreshes a range of rows of said one or more memory banks based on a predetermined value stored in the row address register (col. 8, line 44-53).

With regard to claim 3 and 23 Takemae discloses wherein said row address register stores a predetermined value representative of the maximum row address of said one or more memory banks that receives a write command from said command signals (col. 7, line 47-50).

With regard to claim 4, Takemae discloses wherein said row address register stores a predetermined value representative of the minimum row address of said one or more memory banks that receives a write command from said command signals (col. 7, line 50-52).

With regard to claim 5 and 24, Takemae discloses wherein said row address register stores a predetermined value representative of the maximum row address of said one or more memory banks that receives a write command from the command signals; and said refresh circuit one refreshes rows of the one or more memory banks that have addresses less than or equal to the predetermined value (col. 7, line 47-57) (also with regard to claim 6).

With regard to claim 8 and 18, Takemae discloses wherein said refresh circuit comprises: a refresh address counter (fig. 4, 7a) for incrementing a row address to be refreshed during a refresh cycle; and a controller (fig. 4, 4) that controls access to a row address requested to be refreshed by a refresh request.

With regard to claim 9, 19 and 26, Takemae discloses wherein said refresh circuit performs refreshing as part of an autorefresh operation (col. 3, line 58-col. 4, line 26).

With regard to claim 10, 20 and 27, Takemae discloses wherein said refresh circuit performs refreshing as part of a self-refresh operation (col. 4, line 28-41).

With regard to claim 12, Takemae discloses a memory control system comprising: an inherent memory controller; a memory device (fig. 4) inherently connected to the memory controller via a command bus, wherein command signals are directed from said memory controller to said memory device (it is inherently known in the semiconductor memory art that in every memory system there must be a memory controller controlling the operation of the memory device through the use of a memory controller bus to communicate between the memory controller and the memory device),

wherein the memory device comprising: one or more memory banks (fig. 4, 9); a first row address register (fig. 4, 612); a second row address register (fig. 4, 611); a command decoder (fig. 4, 2) that is connected to said row address register (fig. 4, 61a), and receives said command signals (fig. 4, for example /CS, /RAS, /CAS and /WE) and controls the contents of the row address register; and a refresh circuit (fig. 4, 4 and 7a) connected to said one or memory banks and said row address register, wherein said refresh circuit avoids unnecessary power consumption for refreshing said one or more memory banks (col. 1, line 58-62).

With regard to claim 13, Takemae discloses wherein said refresh circuit only refreshes a range of rows of said one or more memory banks based on a first predetermined value stored in said first row address register and a second predetermined value stored in said second row address register (col. 7, line 47-57) (also with regard to claim 15, 16 and 25).

With regard to claim 14, Takemae discloses wherein said first predetermined value is representative of the maximum row address (fig. 4, 612) of said one or more memory banks that receive a write command from said command signals.

Drafted as Method claim

5. As per claim 28-34 encompass the same scope of invention as to that of claim 1-27 except they draft in method format instead of apparatus format. The claims are therefore rejected for the same reason as set forth above.

Claim Rejections - 35 USC ∋ 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 7, 11 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takemae et al, Pat. No. 6349067 in view of applicant's prior art figure 1.

With regard to claim 7, 11 and 17, as applied in prior rejection, Takemae disclosed all claimed subject matter except wherein said memory controller comprises a normal refresh circuit that sends an autorefresh signal to said memory device via said command bus. However, applicant disclosed in his specification and figure 1 a known computer system having a memory controller (fig. 1, 104) having a normal refresh circuit (applicant's fig. 1, 110) that sends an autorefresh signal to said memory device (fig. 1 102) via said command bus (fig. 1, 106) (see the specification page 3-8). Therefore, it would have been obvious for one having an ordinary skill in the art at the time the invention was made to incorporate a known normal refresh circuit provided within the memory controller to be used by the memory device into Takemae's to direct memory device to operate it's autorefresh operation so that data in the memory device can be refresh.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure. Wright et al (5627791), Floman et al (6857042) and Schreck (6853591) disclose a memory device having refresh circuitry.

8. When responding to the office action, Applicants' are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

9. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1799. The examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 5:30 PM. The examiner's supervisor, David Nelms, can be reached at (571) 272-1787. The fax phone number for this Group is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov should you

have questions on access to the Private Pair system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. Yoha

APRIL 2005

CONNIE C. YOHA
PRIMARY EXAMINER